Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (original) An apparatus comprising:

a real time clock circuit; and

an associated circuit that operates in a first mode when a power supply voltage is present and operates in a second mode when battery power is present, said second mode providing a biasing condition that reduces a sub-threshold off current for the real time clock circuit during battery operation by adjusting source voltage levels for the real time clock circuit.

2. (original) The apparatus of claim 1, wherein the associated circuit comprises one or more switching devices between source and substrate connections of the real time clock circuit.

3. (original) The apparatus of claim 2, wherein the one or more switching devices comprise level shifting logic and one or more multiplexers.

4. (original) The apparatus of claim 1, wherein said adjusting source voltage levels is performed using a battery providing the battery operation.

5. (original) The apparatus of claim 4, further comprising resistors placed across the battery to form bias levels for the biasing condition, wherein said resistors are isolated from the battery during non-battery operation.

6. (original) The apparatus of claim 1, further comprising a power supply ready signal that facilitates isolation of the real time clock circuit during transition from the second mode to the first mode.

7. (original) The apparatus of claim 6, further comprising a delay element that delays the transition from the second mode to the first mode when transitioning back to use of the power supply voltage.

8. (original) The apparatus of claim 7, wherein the delay element comprises a capacitor.

9. (original) The apparatus of claim 1, further comprising decoupling capacitors that inhibit switching induced errors during transition between the first and second modes.

10. (original) A personal computing system comprising:

a core power source;

core power rails coupled with the core power source;

a real time clock circuit coupled with the core power rails;

a battery coupled with the real time clock circuit; and

a bias-mode control circuit that operates in a first mode when the core power source provides power, and operates in a second mode when the battery provides power, said second mode providing a biasing condition that reduces a sub-threshold off current for the real time clock circuit during battery operation by adjusting source voltage levels for the real time clock circuit.

11. (currently amended) The system of claim 10, wherein the bias-mode control circuit ~~associated circuit~~ comprises one or more switching devices between source and substrate connections of the real time clock circuit.

12. (original) The system of claim 11, wherein the one or more switching devices comprise level shifting logic and one or more multiplexers.

13. (original) The system of claim 10, wherein said adjusting source voltage levels is performed using the battery.

14. (original) The system of claim 13, further comprising resistors placed across the battery to form bias levels for the biasing condition, wherein said resistors are isolated from the battery during non-battery operation.

15. (original) The system of claim 10, further comprising a power supply ready signal that facilitates isolation of the real time clock circuit during transition from the second mode to the first mode.

16. (original) The system of claim 15, further comprising a delay element that delays the transition from the second mode to the first mode when transitioning back to use of the power supply voltage.

17. (original) The system of claim 16, wherein the delay element comprises a capacitor.

18. (original) The system of claim 10, further comprising decoupling capacitors that inhibit switching induced errors during transition between the first and second modes.

19. (original) A system comprising:

a real time clock circuit for maintaining a count indicative of real time; and

source-voltage-level adjustment means for operating the real time clock circuit with reduced sub-threshold off current when battery power is present, and for allowing the real time clock circuit to communicate with other computing components when a regular power supply voltage is present.

20. (original) The system of claim 19, wherein the source-voltage-level adjustment means comprises level shifting logic and one or more multiplexers.

21. (original) The system of claim 19, further comprising transition-timing means for isolating the real time clock circuit during power source transitions.

22. (original) The system of claim 19, further comprising capacitor means for inhibiting switching induced errors during power source transitions.

23. (original) A method of operating a real time clock circuit, the method comprising:

operating a real time clock circuit from a power supply during a first mode of operation; and

operating said real time clock circuit from a battery during a second mode of operation that reduces a sub-threshold off current for the real time clock circuit by adjusting source voltage levels for the real time clock circuit.

24. (original) The method of claim 23, wherein operating said real time clock circuit from a battery during a second mode comprises using the battery to perform the adjusting and using resistors placed across the battery to form bias levels for the adjusting, and wherein operating a real time clock circuit from a power supply during a first mode of operation comprises isolating the resistors from the battery during non-battery operation.

25. (original) The method of claim 23, further comprising isolating the real time clock circuit during transition from the second mode to the first mode.

26. (original) The method of claim 23, further comprising delaying transition from the second mode to the first mode when transitioning back to use of the power supply.

27. (original) The method of claim 23, further comprising inhibiting switching induced errors using decoupling capacitors during transition between the first and second modes.